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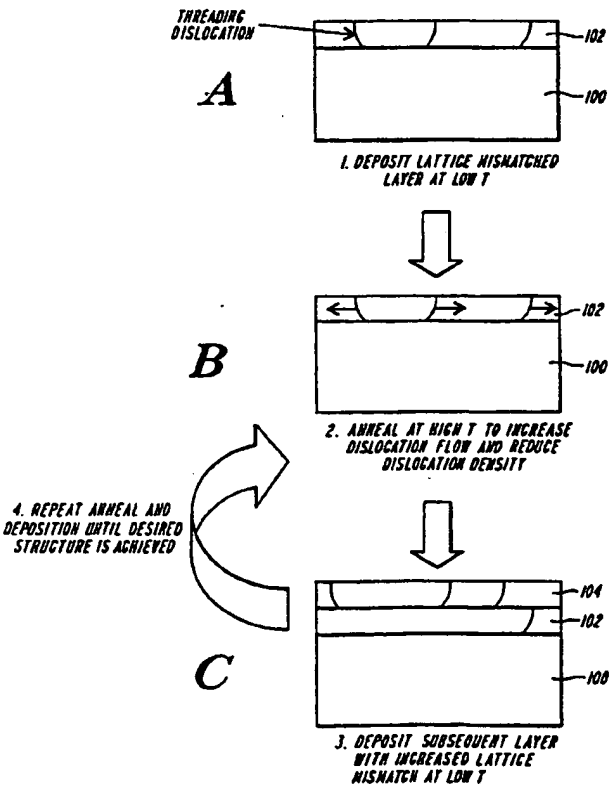

(57) Abstract: A semiconductor structure and method of processing same including a substrate, a lattice-mismatched first layer deposited on the substrate and annealed at a temperature greater than 100°C above the deposition temperature, and a second layer deposited on the first layer with a greater lattice mismatch to the substrate than the first semiconductor layer. In another embodiment there is provided a semiconductor graded composition layer structure on a semiconductor substrate and a method of processing same including a semiconductor substrate, a first semiconductor layer having a series of lattice-mismatched semiconductor layers deposited on the substrate and annealed at a temperature greater than 100°C above the deposition temperature, a second semiconductor layer deposited on the first semiconductor layer with a greater lattice mismatch to the substrate than the first semiconductor layer, and annealed at a temperature greater than 100°C above the deposition temperature of the second semiconductor layer.

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LOW THREADING DISLOCATION DENSITY RELAXED MISMATCHED EPILAYERS WITHOUT HIGH TEMPERATURE GROWTH

PRIORITY INFORMATION

This application claims priority to provisional application Ser. No. 60/177,085 filed January 20 2000.

BACKGROUND OF THE INVENTION

The invention relates to the field of low threading dislocation density relaxed mismatched epilayers, and in particular to such epilayers grown without high temperature.

The goal of combining different materials on a common substrate is desirable for a variety of integrated systems. Specifically, it has been a long-standing desire to combine different semiconductor and oxide materials on a common useful substrate such as a silicon substrate. However, just as the different materials properties are beneficial from the system application perspective, other properties may make such materials combinations problematic in processing. For example, semiconductor materials with different properties often have different lattice constants. Therefore, upon deposition of one semiconductor material on top of another substrate material can result in many defects in the semiconductor layer, rendering it useless for practical application.

Seminal work into the quantitative interpretation of dislocation densities and the connection to growth parameters was accomplished in the early 1990's (see, for example, E.A. Fitzgerald et al. J. Vac. Sci Tech. B 10,1807 (1992)). Using relaxed SiGe alloys on Si as the model system, it was realized that higher temperature growth of compositionally graded layers was a key to producing a relaxed SiGe layer on Si with high perfection.

However, practical constraints from current equipment used to manufacture Si-based epitaxial layers create difficulty in depositing high germanium concentration alloys without deleterious particle formation from either gas phase nucleation or equipment coating. For example, a large amount of current Si-based epitaxial wafers are created using single-wafer, rapid thermal chemical vapor deposition (CVD) systems. Although these systems offer great control of Si epilayer thickness uniformity across a wafer, the process encounters problems when germane is added to the gas stream to deposit SiGe alloy layers. Due to the lower decomposition temperature of germane than silane, dichlorosilane, or trichlorosilane, it is possible to nucleate germanium particles in the gas stream, or to coat parts of the reactor with thick deposits that can lead to particle generation.

The overall effect is that the epitaxial growth on the Si wafer can incorporate many particles, which not only degrade material quality locally, but also act as heterogeneous nucleation sites for additional threading dislocations, decreasing overall material quality. Particle generation occurs more rapidly with higher growth temperature; thus, the growth conditions that lead to lower threading dislocation densities (i.e. higher growth temperatures), unfortunately lead to more particles and a higher threading dislocation density than expected. Lower growth temperatures that avoid higher particle generation will create a higher threading dislocation density.

SUMMARY OF THE INVENTION

The problems of the prior art can be overcome by developing a method to create high dislocation velocities even though deposition occurs at lower growth temperatures. Accordingly, the invention provides a structure and a method to produce a low threading dislocation density, mismatched epilayer without the need for depositing the film at high temperature, thus avoiding the germane particle generation.

In accordance with an embodiment of the invention there is provided a semiconductor structure and method of processing same including a substrate, a lattice-mismatched first layer deposited on the substrate and annealed at a temperature greater than 100°C above the deposition temperature, and a second layer deposited on the first layer with a greater lattice mismatch to the substrate than the first semiconductor layer.

In another embodiment there is provided a semiconductor graded composition layer structure on a semiconductor substrate and a method of processing same including a semiconductor substrate, a first semiconductor layer having a series of lattice-mismatched semiconductor layers deposited on the substrate and annealed at a temperature greater than 100°C above the deposition temperature, a second semiconductor layer deposited on the first semiconductor layer with a greater lattice mismatch to the substrate than the first semiconductor layer, and annealed at a temperature greater than 100°C above the deposition temperature of the second semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1C is a schematic block diagram of the growth process and subsequent structure of low dislocation density, lattice mismatched films using alternating steps of epitaxial growth and high temperature annealing;

Figure 2 is a graph showing the temperature changes and gas flows in a chemical vapor deposition system utilized in accordance with an exemplary embodiment of the

invention;

Figure 3 is a graph showing threading dislocation density at the relaxed SiGe surface vs. growth temperature in SiGe graded layers on Si substrates;

Figure 4 is a graph showing the change in effective strain vs. growth temperature to fit the experimental data with an activation energy of 2.25; and

Figure 5 is a chart showing total and field threading dislocation densities for 20% SiGe on a 0-20% graded buffer (graded at 10% Ge/μm) with and without a high temperature annealing step after growth in which epitaxial growths were performed at 700-750°C.

DETAILED DESCRIPTION OF THE INVENTION

Figures 1A-1C is a schematic block diagram of the growth process and subsequent structure of low dislocation density, lattice mismatched films using alternating steps of epitaxial growth and high temperature annealing. In accordance with an exemplary embodiment of the invention, a relatively low lattice-mismatched film 102 is deposited on a surface of a substrate 100 with a different lattice constant at a low temperature, i.e., where particle generation is at a minimum. A low mismatched film can be defined as one in which the lattice mismatch is less than 1%.

After deposition of the film 102, the film is annealed at high temperature without any deposition source gas flowing across the surface, i.e., hydrogen or nitrogen, since they do not deposit any atoms on the surface. This annealing step increases dislocation flow and nearly completely relaxes the deposited film. Because the mismatch is low, the threading dislocation density remains low. Also, the rapid thermal feature of many CVD reactors is a benefit, since wafer temperature can be changed rapidly with time. If the CVD equipment has a large thermal mass, i.e., in the non-rapid thermal arrangement, this procedure is impractical since the annealing step would require too much time, and therefore increase the cost of manufacturing.

The first two aforementioned steps can be repeated, increasing the lattice mismatch in subsequent layers 104. After this sequence, a relaxed graded composition structure is formed, yet the high temperatures during the growth cycle have been avoided, and therefore the particle problem is minimized.

In the particular case of SiGe alloys deposited on Si substrates, typical growth temperatures in rapid thermal systems are between 600 and 750°C. It is known that near complete relaxation of SiGe layers can be accomplished in this temperature range, with threading dislocation densities on the order of mid-10^5 cm^{-2} to 10^6 cm^{-2}. Although this

density is much lower than the ~10^8 cm^{-2} density achieved with direct growth of the final SiGe layer directly on the Si substrate (without the graded layer), it is generally desired to achieve the lowest threading dislocation density possible. By annealing the layers in-between deposition as described (anneal temperatures greater than 900°C for germanium concentrations less than 50% or so), dislocation densities <mid-10^5 cm^{-2} can be achieved.

The annealing step can be performed after more than one growth step if the lattice mismatch increase is small enough at each interface. However, if fairly large steps (near 1% mismatch) are deposited, an annealing step is required after every growth step.

The process conditions required for the invention are shown in Figure 2, using SiGe alloy deposition as an example. The figure shows growth temperature as well as germane and silane flow versus time for implementation in a CVD system. The temperature is cycled between the growth temperature and the annealing temperature using the rapid thermal feature of the reactor. The key aspect is that the gas is not flowing during the high temperature annealing sequences. Using this method, gas phase nucleation of germane is avoided while still achieving the low dislocation densities associated with high temperature growth.

The use of the invention can be elucidated through the example of the relaxed SiGe/Si system. In this materials system, relaxed SiGe alloys on Si have many useful applications such as high-speed electronics. As can be shown from dislocation kinetics theory in mismatched layers, the rate of lattice mismatch strain relief in a lattice-mismatched film is given by:

$$\frac{\partial \delta}{\partial t} = \frac{\rho_t b}{2} B Y^m \varepsilon_{eff}^m e^{\frac{-U}{kT}} \qquad (1)$$

where δ is the strain relieved by threading dislocation flow (and thereby misfit dislocation creation), ρ_t is the threading dislocation density at the top surface, b is the Burgers vector of the dislocation, B is a constant extracted from dislocation velocity measurements, Y is the biaxial modulus, ε_{eff} is the effective strain in the layer, U is the activation energy for dislocation glide, and T is the temperature of growth.

Realizing that the time derivative of plastic deformation is the 'grading rate' in a graded epitaxial layer, equation (1) can be written in a more practical form for those engineering dislocations in graded structures:

$$\rho_t = \frac{2 R_g R_{gr} e^{\frac{U}{kT}}}{b B Y^m \varepsilon_{eff}^m} \qquad (2)$$

where R_g is the film growth rate and R_{gr} is the film grading rate.

For the particular case of the SiGe graded layer system on Si, the parameters for equation (2) have been extracted experimentally. Figure 3 shows a plot of threading dislocation density vs. temperature for SiGe graded layers grown in a CVD reactor. All relaxed buffers were graded to 30% Ge as a final composition with a 1.5μm final uniform cap layer. It is important to note that threading dislocation densities in graded layers in different CVD reactors have been studied, and it is noted here that the parameters can change slightly with a particular reactor or change in environment cleanliness. However, the numbers shown will not vary significantly, especially on a semilog plot. If an activation energy for dislocation glide is extracted from Figure 3, the result is an activation energy of 1.38 eV.

It is well known that activation energy for dislocation glide in the SiGe system is approximately 2.25 eV and not the extracted value of 1.38 eV. This discrepancy occurs since the extracted value assumes that the effective strain is constant with temperature, when in reality it is not. Thus, if one desires to use the formulations described herein, one must account for the change in effective strain with temperature. Figure 4 is a plot of the effective strain calculated using equation (2) under the assumption that the activation energy for dislocation glide is 2.25 eV. The effective strain drops with increasing growth temperature and is approximately in the $1x10^{-4}$-$3x10^{-4}$ range for growths above 750°C.

It is also clear from Figures 3 and 4 that for growth temperatures equal to or greater than 1000°C, dislocation densities much less than 10^5 cm^{-2} are possible. However, as was stipulated previously, such high growth temperatures using high concentrations of germane in the gas flow (desired for high, economical growth rates) results in disastrous gas phase nucleation.

Using the invention, one can grow at reasonable growth rates at 750°C, avoid gas phase nucleation, but achieve lower threading dislocation densities by annealing at a higher temperature without gas flow. Figure 5 demonstrates the effect annealing can have on dislocation density by summarizing etch-pit density (EPD) measurements for SiGe samples grown with and without a post-cpi, high temperature anneal.

The samples are 20% SiGe layers on SiGe graded buffers graded from 0-20% at a rate of 10% Ge/μm. The threading dislocation densities in the SiGe were measured as grown (growth temperature of 700-750°C), and with a 5 minute anneal at 1050°C performed after growth. As a result of the anneal, the total threading dislocation density decreased from 1.36×10^6 cm^{-2} to 7.25×10^5 cm^{-2}, and the field threading dislocation density decreased from 1.31×10^6 cm^{-2} to 5.48×10^5 cm^{-2}. Incorporating anneals throughout the grading

process as described in this disclosure enables the production of films with total dislocation densities well below 10^5 cm^{-2}.

One can estimate the time that one needs to pause at the annealing temperature (Δt in Fig. 2). This time is determined by ensuring that the dislocations have propagated as far as possible. A conservative estimate of this travel length can be extracted from Figures 3 and 4, with the additional information from x-ray diffraction that samples grown at T > 750C are approximately completely relaxed. The average length of a misfit dislocation (and therefore length a threading dislocation has traveled) is:

$$\lambda_{AVG} = \frac{\rho_\lambda}{\rho_t} = \frac{1}{S\rho_t} = \frac{\delta}{b_{eff}\rho_t} \qquad (3)$$

where ρ_t is the interface dislocation density (inverse of the interface dislocation spacing, S). For the 30% Ge alloy example, $\rho=1.22x10^{-2}$ for complete relaxation. This results in a total misfit length per thread of approximately 5cm using equation 3. Since the experiments were performed on 4-inch (10cm) substrates, it is possible that a significant number are escaping at the edges of the wafer.

It must be remembered that the total length of 5cm is distributed over a number of interfaces in a graded layer. In the case of graded SiGe, typically a graded layer is composed of, for example, 15 layers, each layer with an increment of 2% Ge. If one also imagines a typical grading rate of 10% Ge/μm, each of the 15 layers is 2000Å thick. Thus, each thread is creating about 5cm/15=0.33cm of misfit length in each interface.

Since the expression

$$v = BY^{n_i}\varepsilon_{eff}^{m_i}e^{\frac{-U}{kT}} \qquad (4)$$

estimates the dislocation velocity, the minimum time (Δt) to ensure close to maximum relaxation is:

$$\Delta t = \frac{\lambda}{v} \approx 0.1 \text{ seconds} \qquad (5)$$

where it is assumed that annealing occurs at 1100C. Thus, the annealing time required at the elevated temperature need not be longer than a matter of seconds to ensure that the layer or layers grown at the reduced temperature have traveled their maximum length and created the lowest possible threading dislocation density. This calculation verifies that the invention is well suited to a CVD reactor with a low thermal mass in the substrate area, such as a rapid thermal CVD system.

A structure and method for creating relaxed mismatched films with low threading

dislocation density, by avoiding growth during high temperature cycles and thus avoiding particle nucleation in rapid thermal CVD systems has been described. The particular case of SiGe/Si has been used to exemplify the growth sequence and parameters. However, the invention can also be utilized to lower defect densities in the compositional grading of other materials such as InGaAs and InGaP.

Although the invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A semiconductor structure comprising:

a substrate;

a lattice-mismatched first layer deposited on said substrate and annealed at a temperature greater than 100°C above the deposition temperature; and

a second layer deposited on said first layer with a greater lattice mismatch to said substrate than said first layer.

2. The semiconductor structure of claim 1, wherein said substrate comprises Si and said first and second layers comprise $Si_{1-x}Ge_x$.

3. The semiconductor structure of claim 1, wherein said substrate has a surface layer comprising Si and said first and second layers comprise $Si_{1-x}Ge_x$.

4. The semiconductor structure of claim 1, wherein said substrate comprises GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

5. The semiconductor structure of claim 1, wherein said substrate has a surface layer comprising GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

6. The semiconductor structure of claim 1, wherein said substrate comprises GaP and said first and second layers comprise $In_zGa_{1-z}P$.

7. The semiconductor structure of claim 1, wherein said substrate has a surface layer comprising GaP and said first and second layers comprise $In_zGa_{1-z}P$.

8. The semiconductor structure of claim 2, wherein said first and second layers differ by a Ge concentration less than 10% Ge.

9. The semiconductor structure of claim 2, wherein said first and second layers differ in Ge concentration by approximately 1.5% Ge.

10. The semiconductor structure of claim 2, wherein said first and second layers of $Si_{1-x}Ge_x$ are deposited at a growth temperature less than 850°C.

11. The semiconductor structure of claim 2, wherein said annealing occurs at a temperature greater than 900°C.

12. The semiconductor structure of claim 2, wherein anneal time is greater than 0.1 seconds.

13. The semiconductor structure of claim 2, wherein said first and second layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C.

14. The semiconductor structure of claim 2, wherein said first and second layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C, and the anneal time is greater than 0.1 seconds.

15. The semiconductor structure of claim 1, wherein said lattice-mismatched semiconductor layer is deposited by chemical vapor deposition.

16. A semiconductor graded composition layer structure on a semiconductor substrate comprising:

a semiconductor substrate;

a first semiconductor layer having a series of lattice-mismatched semiconductor layers deposited on said substrate and annealed at a temperature greater than 100°C above the deposition temperature;

a second semiconductor layer deposited on said first semiconductor layer with a greater lattice mismatch to said substrate than said first semiconductor layer, and annealed at a temperature greater than 100°C above the deposition temperature of said second semiconductor layer.

17. The structure of claim 16, wherein said substrate comprises Si and said first and second layers comprise SiGe.

18. The structure of claim 16, wherein said substrate has a surface layer comprising Si and said first and second layers comprise $Si_{1-x}Ge_x$.

19. The structure of claim 16, wherein said substrate comprises GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

20. The structure of claim 16, wherein said substrate has a surface layer comprising GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

21. The structure of claim 16, wherein said substrate comprises GaP and said first and second layers comprise $In_zGa_{1-z}P$.

22. The structure of claim 16, wherein said substrate has a surface layer comprising GaP and said first and second layers comprise $In_zGa_{1-z}P$.

23. The structure of claim 17, wherein sequential layers in the graded composition layers differ by a Ge concentration less than 10% Ge.

24. The structure of claim 17, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5% Ge.

25. The structure of claim 17, wherein said first and second layers are deposited at a growth temperature of less than 850°C.

26. The structure of claim 17, wherein said annealing occurs at a temperature greater than 900°C.

27. The structure of claim 17, wherein anneal time is greater than 0.1 seconds.

28. The structure of claim 17, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C.

29. The structure of claim 17, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately

1050°C, and the anneal time is greater than 0.1 seconds.

30. The structure of claim 16, wherein said lattice-mismatched semiconductor layer is deposited by chemical vapor deposition.

31. A method of processing a semiconductor structure comprising:

providing a substrate;

depositing a lattice-mismatched first layer on said substrate;

annealing said first layer at a temperature greater than 100°C above the deposition temperature; and

depositing a second layer on said first layer with a greater lattice mismatch to said substrate than said first layer.

32. The method of claim 31, wherein said substrate has at least a surface layer comprising Si and said first and second layers comprise $Si_{1-x}Ge_x$.

33. The method of claim 31, wherein said substrate has at least a surface layer comprising GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

34. The method of claim 31, wherein said substrate has at least a surface layer comprising GaP and said first and second layers comprise $In_zGa_{1-z}P$.

35. The method of claim 32, wherein said first and second layers differ by a Ge concentration less than 10% Ge.

36. The method of claim 32, wherein said first and second layers differ in Ge concentration by approximately 1.5% Ge.

37. The method of claim 32, wherein said first and second layers of $Si_{1-x}Ge_x$ are deposited at a growth temperature less than 850°C.

38. The method of claim 32, wherein said annealing occurs at a temperature greater than 900°C.

39. The method of claim 32, wherein anneal time is greater than 0.1 seconds.

40. The method of claim 32, wherein said first and second layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C.

41. The method of claim 32, wherein said first and second layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C, and the anneal time is greater than 0.1 seconds.

42. The method of claim 31, wherein said lattice-mismatched semiconductor layer is deposited by chemical vapor deposition.

43. A method of processing a semiconductor graded composition layer structure on a semiconductor substrate comprising:

providing a semiconductor substrate;

depositing a first layer having a series of lattice-mismatched semiconductor layers on said substrate;

annealing said first layer at a temperature greater than 100°C above the deposition temperature;

depositing a second layer on said first layer with a greater lattice mismatch to said substrate than said first layer; and

annealing said second layer at a temperature greater than 100°C above the deposition temperature of said second layer.

44. The method of claim 43, wherein said substrate has at least a surface layer comprising Si and said first and second layers comprise $Si_{1-x}Ge_x$.

45. The method of claim 43, wherein said substrate has at least a surface layer comprising GaAs and said first and second layers comprise $In_yGa_{1-y}As$.

46. The method of claim 43, wherein said substrate has at least a surface layer comprising GaP and said first and second layers comprise $In_zGa_{1-z}P$.

47. The method of claim 44, wherein sequential layers in thc graded composition layers differ by a Ge concentration less than 10% Ge.

48. The method of claim 44, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5% Ge.

49. The method of claim 44, wherein said first and second layers are deposited at a growth temperature of less than 850°C.

50. The method of claim 44, wherein said annealing occurs at a temperature greater than 900°C.

51. The method of claim 44, wherein anneal time is greater than 0.1 seconds.

52. The method of claim 44, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the anneal temperature is approximately 1050°C.

53. Thc method of claim 44, wherein sequential layers in the graded composition layers differ in Ge concentration by approximately 1.5%, the growth temperature is approximately 750°C, and thc anneal temperature is approximately 1050°C, and the anneal time is greater than 0.1 seconds.

54. The method of claim 43, wherein said lattice-mismatched semiconductor layer is dcposited by chemical vapor deposition.

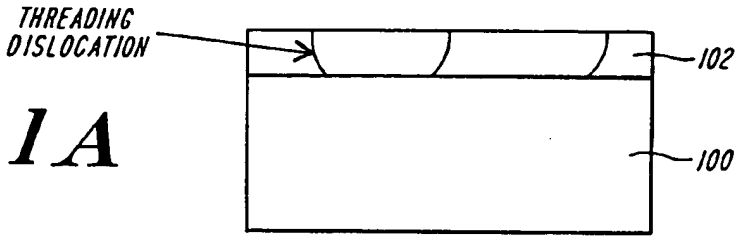

FIG. 1A

1. DEPOSIT LATTICE MISMATCHED LAYER AT LOW T

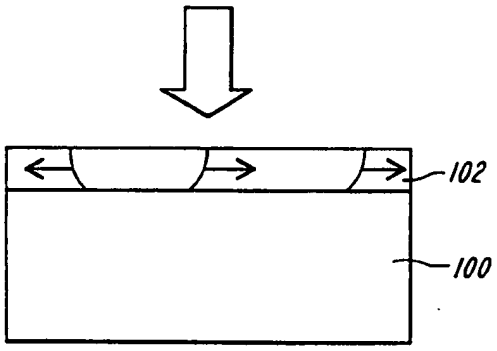

FIG. 1B

2. ANNEAL AT HIGH T TO INCREASE DISLOCATION FLOW AND REDUCE DISLOCATION DENSITY

4. REPEAT ANNEAL AND DEPOSITION UNTIL DESIRED STRUCTURE IS ACHIEVED

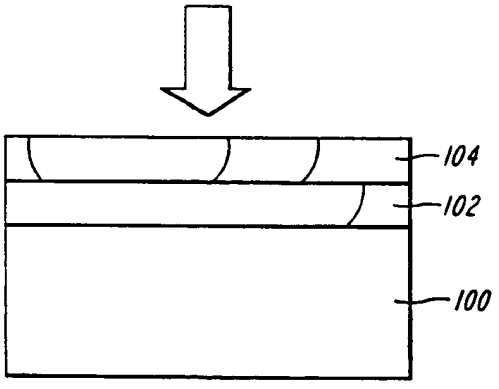

FIG. 1C

3. DEPOSIT SUBSEQUENT LAYER WITH INCREASED LATTICE MISMATCH AT LOW T

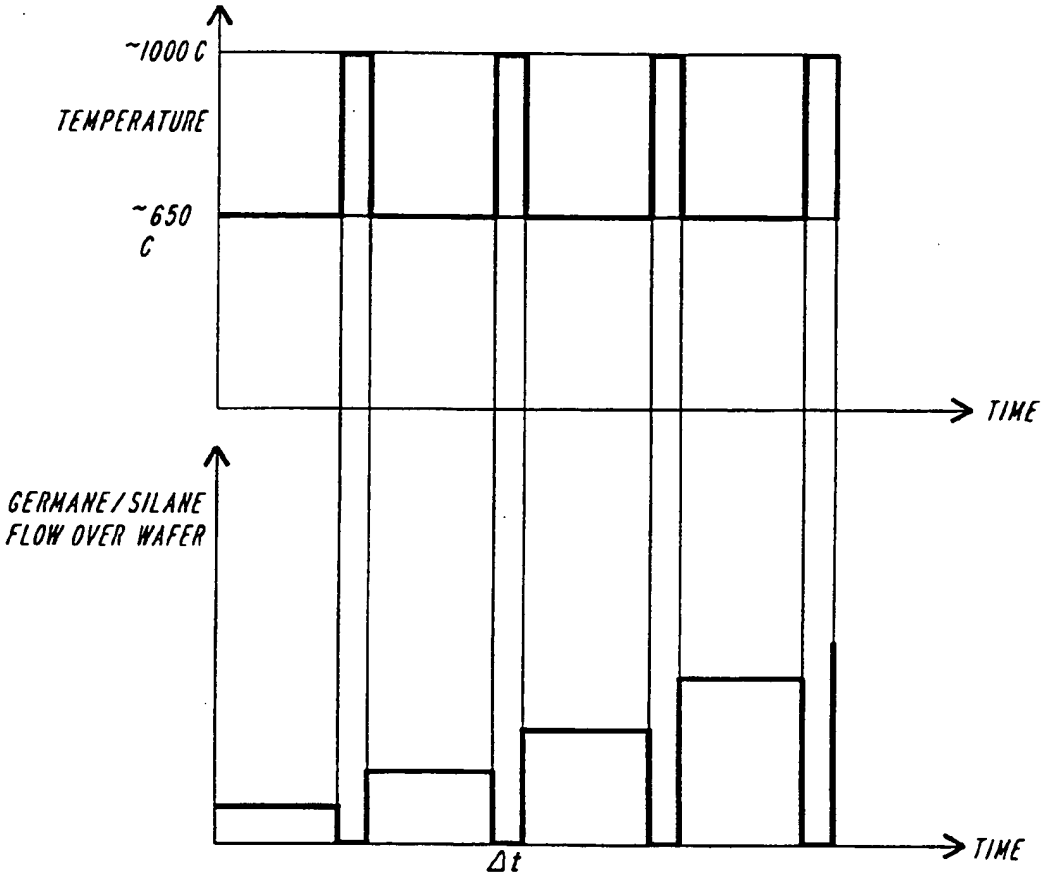
~1000 C
TEMPERATURE
~650 C
TIME
GERMANE/SILANE FLOW OVER WAFER
TIME
Δt

FIG. 2

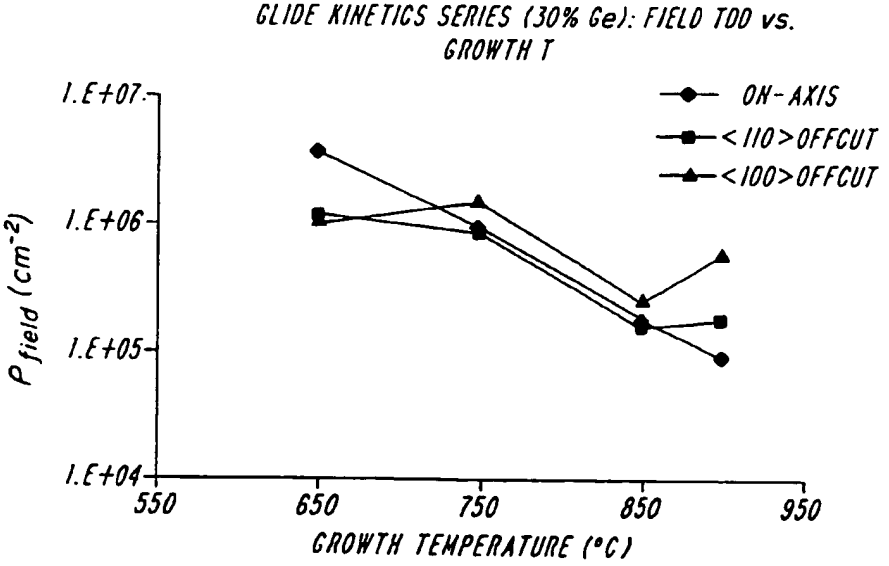
GLIDE KINETICS SERIES (30% Ge): FIELD TOO vs. GROWTH T
ON-AXIS
<110>OFFCUT
<100>OFFCUT
1.E+07
1.E+06
1.E+05
1.E+04
P field (cm-2)
550
650
750
850
950
GROWTH TEMPERATURE (°C)

FIG. 3

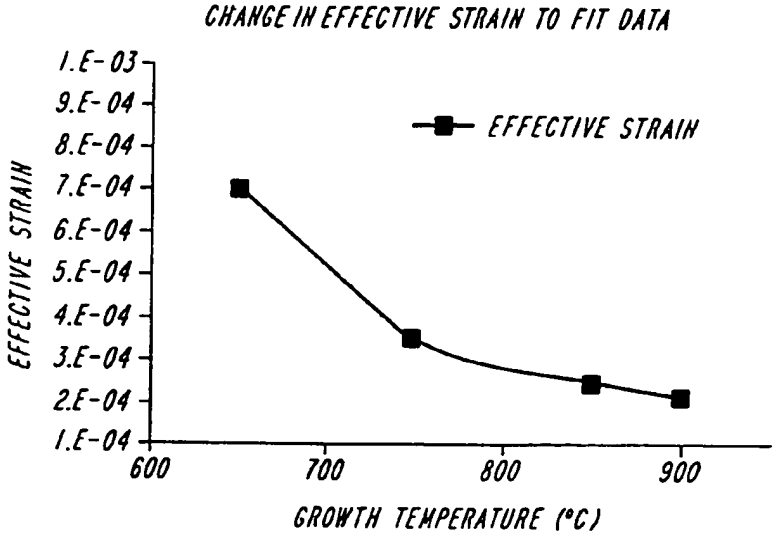

FIG. 4

Sample	Total Threading Dislocation Density (# / cm^2)	Field Threading Dislocation Density (# / cm^2)
20% SiGe on Si with graded buffer as grown	1.36×10^6	1.31×10^6
20% SiGe on Si with graded buffer after a 5 min anneal at 1050°C	7.25×10^5	5.48×10^5

FIG. 5

INTERNATIONAL SEARCH REPORT

Internatic Application No
PCT/US 01/01413

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 279 687 A (GIBBINGS CHRISTOPHER J ET AL) 18 January 1994 (1994-01-18)	1-7, 10-12, 31-34, 37-39,42
Y	column 2, line 44 -column 4, line 21 column 6, line 51 -column 7, line 2 claims 1,4	8,9,13, 14, 16-30, 35,36, 40,41, 43-54

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
21 May 2001	29/05/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Giordani, S

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